```
User name:    SHAW (11)                    Queue:  UIDESK/UNIX_UIMKGT
File name:                                 Server: CLFPCD010
Directory:
Description: nordic_2.txt
             December 21, 1998                              6:35pm
```

EXHIBIT
RX-573

```
 SSS  H   H   A   W   W
S   S H   H  A A  W   W
S     H   H A   A W   W
 SSS  HHHHH A   A W W W
    S H   H AAAAA W W W
S   S H   H A   A WW WW
 SSS  H   H A   A W   W


L      SSS  TTTTT
L     S   S   T
L     S       T    : :
L      SSS    T    : :
L         S   T
L     S   S   T    : :
LLLLL  SSS    T    : :
```

Engineering Specification

* * * * *

Nordic – Register Definitions

General Information, Definitioins and Notes that apply to this document

General:

1. SRxy with odd x, and 0 or 1 y are not allowed as they overlap with h/w cursor and icon registers.

Definitions:

1. In this document "h/w cursor" = "graphics cursor"

Notes:

CL 158140

Prepared by: _____

Approved by: _____

CL 158142

1.0 Nordic Special Registers

1.1 SR7 - Extended Sequencer Mode

Bit	Definition
[7:0]	Like in AVGA3 (not like in T1)

1.2 SRF - DRAM Control

Bit	Definition
[6]	Disable Video Memory fast-page mode for CPU cycles
[5]	CRT FIFO 16x32 Depth Selection (default: 8x32)
[7,4,3]	Video Memory Width and structure: 000 = 32bit, 4 x 512K x 8 001 = 16bit, 1 x 256k x 16 010 = 32bit, 2 x 256K x 16 (default) 011 = reserved for 64bit 100 = 32bit, 4 x 256k x 16, two banks 101:111 reserved
[2]	Short RAS Timing 3.5/2.5 (default: Long RAS Timing 4/3)
[1]	Assymetric DRAM support (default: symetric DRAM support) %
[0]	Two CAS 16bit 256Kx16 Memory Chip (default: two WE) %

1.3 SR16

Bit	Definition
[7]	Disable driving CPU Data Bus during first T2 in VL bus or local bus. To be used with 20MHz 486DX or DX2 bus with zero wait states. Default (reset state) = 1 This bit allows to optimize chip response for slow buses, reducing the number of wait states.
[6]	RDY DLY for I/O in all buses. Default (reset state) = 1
[5:0]	As in 5428 Reference Manual.

0.1 SR18 Signature Generator Control Register

This register is used to control and read-back the status of Nordic signature generators. There are two signature generators in Nordic: one for the data path, that can be applied to either VGA data path or to the MVA data path, and one on the dither, NTSC and shader - the panel data path.

Bit	Definition
[7]	**Enable Panel Signature Generator (default = 0)**
[6]	**Reserved - see 5428 Tech Ref. It should do the same thing**
[5]	Enable Data Generator for the "Video Data Path" signature generator. **Once Data Generator is Enabled, this bit becomes Signature generator read-back bit until the enable is reset by SR18[1].** **CR3D[7] selects the data path for the signature generator: VGA or MVA.**
[4:2]	Pixel Bus Select [2:0]
[1]	Reset Signature Generators: this bit resets all the signature generators in Nordic
[0]	Signal Generator Enable/Status

Only bits 7 and 6 are new in Nordic, but bit 1 has extended functionality.

0.1 SR21 (SR1A in 62XX moved to SR21 in Nordic)

Bit	Definition
[7]	One Refresh per Scanline Select bit
[6]	Dual Scan Color STN select bit, requires CR1C panel type bits to point to STN panels[6] Dual Scan Color STN select bit, requires CR1C panel type bits to point to STN panels
[5]	Reduce CPU Latency by adjusting Half Frame Buffer FIFO Threshold with Monochrome Dual STN panels[5] Reduce CPU Latency by adjusting Half Frame Buffer FIFO Threshold with Monochrome Dual STN panels
[4]	reserved ??
[3]	reserved ??
[2]	Enable test bus to come out to LD,UD, R5 and R4.
[1:0]	Select one of the four available test bus branches to be outputed by the chip. This bits are to be used by manufacturing test.

1.4 SR22 - h/w Configuration (read only)

Bit	Definition
[7]	32bits PCI bus no Burst h/w PU configuration on MD24. It is called "PCINBPU" (read only bit). This is a reserved configuration in case burst does not work on a PCI bus (this bit was SR2A[0]). On MD23 - PCINBPU.
[6]	8bit BIOS (default 16bit BIOS) On MD22 - BIOS8PU. In ISA bus configuration the BIOS is always supported.
[5]	46e8[3] sleep (default 3c3 sleep) Nordic-1M comes up awake. We need to clear this with the BIOS and driver group. On MD21 - S46PU.
[4]	Reserved
[3]	select external clocks: MCLK and VCLK on SW0/MCLK/XMCLK and OSC/XVCLK. (default: internal clock synthesizer, SW1 and OSC) 0 = internal clocks with the pins used as inputs for panel type switch #1 and OSC. If SR23[4] and SR23[0] are 1, VCLK and SW0/MCLK/XMCLK, respectively become VCLK and MCLK outputs respectively, for testpurposes (only if SR22[3]=0 MCLK can be seen, but VCLK can be seen even if SR22[3]=1 as long as SR23[4]=1) 1= SW0/MCLK/XMCLK and OSC/XVCLK become XMCLK and XVCLK inputs generating directly chip MCLK and VCLK without clock synthesizer. The clock synthesizers are powered down if SR22[3]=1. This is CF[4] in AVGA3. On MD19 - XCLKPU.
[2]	VESA VL bus 50MHz On MD18 - FVLPU.
[1]	Select ISA bus support (default: 33MHz or less VESA VL) On MD17 - ISAPU **If this bit is 1**, Nordic is in ISA bus configuration and EBROMn/SLEEPIn pin is EBROMn output to the BIOS ROM and the BIOS decode at C000:0 is operational. **If this bit is 0**, EBROMn/SLEEPIn pin is SLEEPIn input and can be used to put the chip to sleep (not present on the CPU bus - the same effect as 3C3 or 46E8 but from a pin).
[0]	Select PCI bus support (default: 33MHz or less VESA VL) On MD16 - PCIPU.

1.5 SR23 - s/w configuration #1

Bit	Definition
[7]	Enable FCVCLK to drive the internal RAMDAC
[6]	SBY/ACTI select bit Default: SBY on SBY/ACTI pin.
[5]	Suspend/BLI select bit Default: 0 = Suspend pin 1 = Back-Light Input pin
[4]	Enable Output Internal VCLK on VCLK/FCDCLK Default: 0 = Output Constant Level L If SR23[4] = 1, VCLK is outputed on VCLK/FCDCLK pin independent on SR22[3] (external/internal clock selection). VCLK can be output also on the Feature Conector.DCLK, if the Feature Connector is enabled . Only there is an option to output VCLK/2 on FCDCLK.
[3]	Enable Pixel Semi. 2070 I/O Decode on LDEVn Default: 0 = I/O address 27C0:27C9 are not decoded by Nordic on LDEVn 1 = I/O address 27C0:27C9 are decoded by Nordic on LDEVn (this bit was on 32KHz/OVRW selection which is no longer needed)
[2]	48KB BIOS (default: 32KB of BIOS, when BIOS enabled)
[1]	ZERO Wait state for BIOS in ISA (default: one wait state?)
[0]	Output MCLK on SW0/MCLK/XMCLK pin if SR22[3]=0. Default: 0= SW0/MCLK/XMCLK is an input, namely SW0 = input, if SR22[3] = 0 XMCLK= input, if SR22[3] = 1

1.6 SR24 - Panel Type Switches

Bit	Definition
[7]	VAFCPU (VESA Advanced Feature Connector External Pull-up) Read-back. Read only bit. If external pull-up (the bit read-back = 1), then all VAFC pins are configured for Video Port. Otherwise, they have other functions, or are disabled if no other function. (Disabled = the inputs are foced to the TTL and CMOST threshold, controls are off & the outputs are high-Z. It actually reads back what is latched on Reset on VAFCPU. On MD25 - VAFCPU.
[6]	Compressed Live Video Enable bit (SashaPack enable) (default: disable)
[5]	Reseved ~~(for Audio IN enable bit)(from CS4215 to Nordic). (default: disable).~~
[4]	Reserved ~~(for Audio Out enable bit) (from Nordic to CS4215). (default: disable).~~
[3]	All external Pull-Ups s/w controlled read (on a 1->0 transition) This bit is needed for restore operation if total graphics controller power off is used. Also, if the reset is too short to read the switches which have large resitence PU/PD, this bit can help. SW2:0 are directly read on the I/O bus (no latchat reset). So they do not need s/w read for save/restore.
[2:0]	SW2:0 pins read back (read only bits)

1.7 SR25 - Timers S/W Reset, H/W Config. #2 & Packed Modes Register

Bit	Definition
[7]	This bit replaces CF2 (MD18) of 5428. If this bit is set, the internal DAC will respond to 8514 DAC Address 2EA-2ED in addition to the standard VGA DAC addresses.This bit is reset to zero (default: 0= Standard VGA DAC address).
[6]	This bit replaces CF0 (MD16) of 5428. It allows to work with an external RAM-DAC. It uses EBROM output as External RAMDAC Address Select for I/O while it still decides C000 for memory reads when in ISA. This is a feature of 5428 which we chose not to take out for the time being.This bit is reset to zero. Default = 0; Standard VGA DAC address.
[5]	Enable 1bit/pixel packed mode
[4]	Reserved for "Enable 2bit/pixel packed mode"
[3]	Enable 4bit/pel packed mode
[2]	Faster PCI bus for memory write (1mclk less to wait)
[1]	Reset Standby Timer (moved from T1 SR8[5])
[0]	Reset Backlight Timer (moved from T1 SR8[4])$$$

1.8 SR26 - Least-Significant Byte of Shader Signature

Bit	Definition
[7:0]	

1.9 SR27 - Most-Significant Byte of Shader Signature

Bit	Definition
[7:0]	

1.10 SR28:SR29 - New Easy to Access BIOS Scratch Registers #5 & #6

Bit	Definition
[7:0]	**Notes on Scratch Registers:** 1. There are 13 18bit scratch registers available in the RAMDAC RAM. They can be accessed by programmimg SR12[1]=1. They are accessed as any RAMDAC RAM register (in groups of 3 I/O accesses). 2. Please note that SR9 and SRA are AVGA3 and T1 Scratch Registers #1 and #2. Also SR14 and SR15 are AVGA3 Scratch Registers #3 and #4 (not in T1).

2.0 H/W Icon Registers

H/W Icon Horizontal and Vertical position are programmed exactly like the h/w cursor position.
SR12[3]=1 will make this mechanism address h/w icon.
SR12[3]=0 will make this mechanism address h/w cursor.

Note: In this document "h/w cursor" = "graphics cursor"

2.1 SR10,30,50,70,90,B0,D0,F0 - H/W Icon & Cursor Horizontal Position

Bit	Definition
[7:0]	

2.2 SR11,31,51,71,91,B1,D1,F1 - H/W Icon & Cursor Vertical Start Position

Bit	Definition
[7:0]	

2.3 SR12 - Graphics Cursor Attributes Register *(Nordic added bit 3)*

Bit	Definition
[7]	Overscan Color Protect
[6]	Tristate all Video Memory Pins (address, data, RAS,CAS,WE,OE) 0 = no tri-state 1 = tri-state Can be used to share Video Memory with a second graphics controller. The memory contents may be lost when switching.
[5:4]	Reserved
[3]	This bit selects CPU access for Icon-position modification versus h/w-cursor position (both horizontal and vertical). As for h/w cursor, for h/w icon the horizontal position effect is gated by the vertical position update [7:0] Coarse Horizontal Position (in character clocks). Select CPU Access to h/w icon position update both horizontal and vertical). Default = 0 = h/w cursor CPU access. This bit does not affect SR2A[6] and SR2E[0] which are always accessible by the CPU.
[2]	Cursor Size Select (32 x 32 or 64 x 64)

[1]	Allow CPU Access to DAC Extended Colors
[0]	Graphics Cursor Enable

2.4 SRX - Sequencer Register Index

Bit	Definition
[7:5]	These bits select the low-order bits of vetical position; i.e., the **fine position** (in VCLK). Since h/w **cursor** works only in graphics, three bits are enough in most cases for an 8-dot character clock. However, h/w **icon** needs more fine bits, since it works in text which can be an 8, 9 or 10-dot character clock. **SR2A[6]** is the **msb** for fine position for h/w **icon**, to be used with 9 and 10-dot fonts. Actually, h/w cursor needs to be positioned within ten dots when horizontal expansion from 640-to-800 is on. **SR2E[0]** is the **msb** for fine position for h/w **cursor.** To speed up writing this register bit, no other bit of SR2E will be used.
[7:0]	Corase Vertical Position (in scan lines).

2.5 SR2A - H/W Icon #0 Control Register

Bit	Definition
[7]	**Icon Test Bit.** When this bit = '1', it enables Icon test mode.Relevant icon control signals are placed on the test bus. Default = 0.
[6]	**Icon Horizontal Fine-Position Most-Significant Bit[3].** To be used with 9 and 10-dot character clocks, when in text or in horizontally expanded graphics. Since h/w icon position is seldom updated, no effort was made to minimize s/w needed to write this icon position bit.
[5]	**Memory Map Selection for Icon #0** '0' = map zero, '1' = map one)
[4]	**Enable Vertical-Scan-Line Doubling for Icon #0.** When enabled, the icon extends down and pushes all the other icons down. When this bit = '1', the icon #0 displays 128 scan lines, but each scan line is replicated.
[3]	**Enable Horizontal Pixel Doubling for Icon #0.** When this bit = '1', the icon #0 displays 128 pixels, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #0** '1' = blink at half text-cursor blink rate.
[1]	**Display mode selection for Icon #0:** 3colors + transpency or 4 colors '0' = four colors, '1' = three colors + transparent, '00' = transparent The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	Icon #0 Display Enable: Default = '0'

2.6 SR2B - H/W Icon #1 Control Register

Bit	Definition
[7:6]	Reserved
[5]	**Memory Map Selection for Icon #1** '0'= map zero, '1' = map one)
[4]	**Enable Vertical-Scan-Line Doubling for Icon #1.** When enabled, the icon extends down and pushes all the other icon down. When this bit = '1', the icon displays 128 scan lines for icon #1, but each scan line is replicated.
[3]	**Enable Horizontal-Pixel Doubling for Icon #1.** When this bit = '1', the icon displays 128 scan lines for icon #1, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #1**
[1]	**Display Mode Selection for Icon #1:** 3colors + transpency or 4 colors '0' = four colors, '1' = three colors + transparent, '00' = transparent The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	**Icon #1 Display Enable**: Default = '0'

2.7 SR2C - H/W Icon #2 & PCI Byte Swap Control Register

Bit	Definition
[7]	Enable PCI bus base register 14H, bits 31:24 as defining a valid address range for Nordic. Valid only with PCI bus. 0= 14H base address contents is not decoded as a valid address range 1= 14H base address is decoded as a valid address range
[6]	Enable byte swap in the address space specified by PCI base address 14H bits 31:24. Byte zero becomes byte 1 and byte 2 becomes byte 3 and vice-versa (byte 1 becomes byte 0 and byte 3 becomes byte 2). Valid only with PCI bus.
[5]	**Memory Map Selection for Icon #2** '0' = map zero, '1' = map one)
[4]	**Enable Vertical Scan Line Doubling for Icon #2.** When enabled, the icon extends down and pushes all the other icons down. When this bit = '1', the icon displays 128 scan lines for icon #2, but each scan line is replicated.
[3]	**Enable Horizontal Pixel Doubling for Icon #2.** When this bit = '1', the icon displays 128 pixels for icon #2, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #2**
[1]	**Display Mode Selection for Icon #2:** 3colors + transpency, or 4 colors '0' = four colors, '1' = three colors + transparent, '00' = transparent. The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	**Icon #2 Display Enable:** Default = '0'

2.8 SR2D - H/W Icon #3 Control Register

Bit	Definition
[7:6]	Reserved
[5]	**Memory Map Selection for Icon #3** '0' = map zero, '1' = map one)
[4]	**Enable Vertical Scan Line Doubling for Icon #3.** When enabled, the icon extends down and pushes all theother icons down. When this bit = '1', the icon displays 128 scan lines for icon #3, but each scan line is replicated.
[3]	**Enable Horizontal Pixel Doubling for Icon #3.** When this bit = '1', the icon displays 128 pixels for icon #3, but each pixel is replicated horizontally. The icon extends towards right as we look at it.
[2]	**Enable Blink for Icon #3**
[1]	**Display mode selection for Icon #3:** 3colors + transpency or 4 colors (0 = four colors, 1 = three colors + transparent, 00 = transparent) The h/w icon is always two bits per pixel. This bit controls how these two bits are used.
[0]	**Icon #3 Display Enable:** Default = '0'

2.9 SR2E - Graphic-Cursor Horizontal-Position Extension Register

Bit	Definition
[7:1]	Not Used: These bits should not be used for anything but additional fine position bits for graphic cursor. This way, no masking has to be done in order to write bit [0] of this register. Since the cursor is written all the time, it is important to leave these register bits not used.
[0]	Bit[3] of Horizontal Fine Position for Graphic Cursor Together with SRX[7:5] as bits[2:0] this bits define the horizontal fine position. This bit should be used with 10 bit character clock (normally used with 800 x 600 panels when expanding horizontally a 640 dots image).

3.0 Panel Format and Control Registers

R0x and R1x are reserved (not used like in 62xx)

Horizontal CRTC Registers Shadowing

In order to run VGA programs on 800x600 panels, Nordic needs to shadow the horizontal timing registers except the display enable end, which is application dependent.
(T1 has shadows only for horizontal total.)
This is because all horizontal timing registers but HDE have to be set-up for 800x600 in order to run an 800x600 panel. Symulscan with 800x600 panels runs even the CRT as an 800x600 display in all graphics modes.
In T1 as well as in Nordic, vertical panel registers are mapped at R2x, R3x,... accesible when CR2D[7] = 1. In nordic these registers remain there.
IN T1 there are two registers: **R0x and R1x** which represent HTot shadows, accessible with **CR2D[7]**. They are no longer used in Nordic, **but there is a replacement for them, independent of CR2D[7].**

In Nordic, H Total, H Retrace Start and End, H Blank Start and End are shadowed. Each entity has two values to chose from: a value for dclk/2 and a value for dclk not divided by two. The effect selection is done automatically based on SR1[3] value, but for access there is a selection bit: CR2C[4] to control which of the two sets of registers gets read or written.
Here is a summary of the horizontal shadow registers and its controls:
CR2C[5] write protect for horizontal shadow:
1 -> write both the shadow registers and the correwsponding standard VGA registers fields (some registers are not accessed entierly but only in their timing part)
read back the shadow registers

0 -> write only the standard horiz. timing VGA registers (the shadow registers are write protected). Changing onlt the value of these registers does not have any effect over the CRTC timing.
read back the standard VGA horiz. timing registers
CR2C[4] Select the set of horizontal timing shadow registers to be used (low rez or normal). This bit is reutilsed from T1: it was low power RAMDAC mode - tie now the logic L) .
0 -> select Ry for access
1 -> select Rz for access

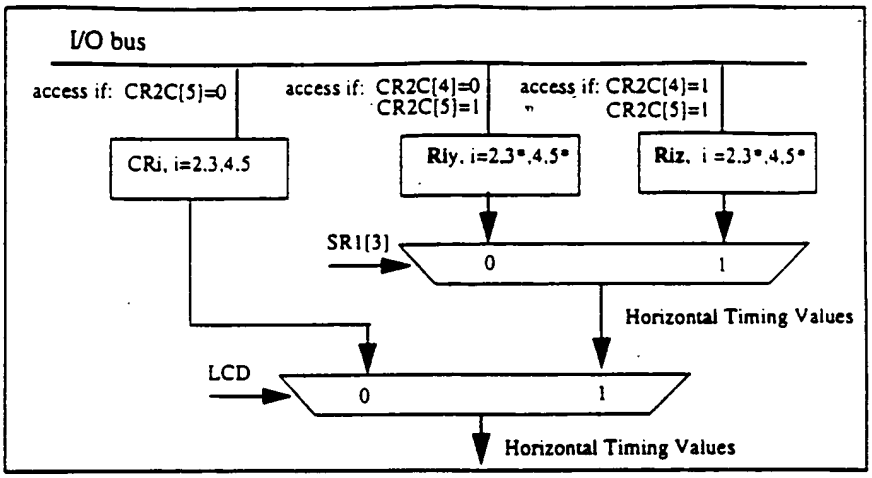
To diferentiate from the Rx registers which still exist as in T1, and are vertical panel registers, we'll call the two sets of horizontal shadows mapped in the same address space Ry and Rz (Ry = normal, Rz = dclk/2 case)
The effect of Ty and Rz is controlled by SR1[3] (dclk/2 bit).

The Horizontal Timing shadow registers are:
R0y,z R02y,z R03y,z (only lower bits) R04y,z R05y,z (only lower bits)

When CR2D[7] =1 we can access only the panel registers: R2x,... RBx. In this case we cannot access either the VGA standard registers or the horizontal timing shadow registers. **Please note that R0x and R1x are reserved in Nordic. Their function is replaced by R0y,z.**

Standard VGA CR0,2,3,4,5 horizontal timing registers (only the timing fields) do not have any effect on the CRTC: only the shadow registers have effect.

See also CR2D and CR2C description.



3.1 R9x - TFT Panel Data Format & Panel Size

Bit	Definition
[7]	Reserved
[6:4]	Select a 0 to 7 shift-clock delay from the internal character clock counter (8 VCLK/ Character Clock) to TFT panel HSYNC (LLCLK) signal; as in T1.
[3:2]	Panel Size: '00' = 640 x 480 '01' = 800 x 600 '10' = 1024 x 768 '11' = 1280 x 1024 Please note that Nordic supports only 640 x 480 and 800 x 600 STN and TFT panels.
[1:0]	TFT Panel Type: '00' = 9-bit (333); as in T1 '10' = 12-bit (444); as in T1 '01' = 18-bit (666); was x1 in T1 covering both '01' and '10' !! '11' = 24-bit (888); new in Nordic

3.2 The following registers, RCx, RDx, REx are additions for 800x600 panels, to R3x, R4x and R5x "LFS Vertical Counter Value Compare" and help with vertical automatic centering on these panels.

RCx - LFS Vertical Offset Register for 600 lines modes

Bit	Definition
[7:0]	LFS signal least significant bits for 600 lines panel & 600 lines mode or any mode-

	that is vertically expanded to 600 lines. Write protected by CR2D[7].

3.3

RDx - LFS Vertical Offset Register for 525 lines modes

Bit	Definition
[7:0]	LFS signal least significant bits for 600 lines panel & 525 lines mode or any mode vertically expanded to 525 lines (like modes 10 and F that have 350 lines). Write protected by CR2D[7].

3.4

REx - Overflow bits for RCx and RDx

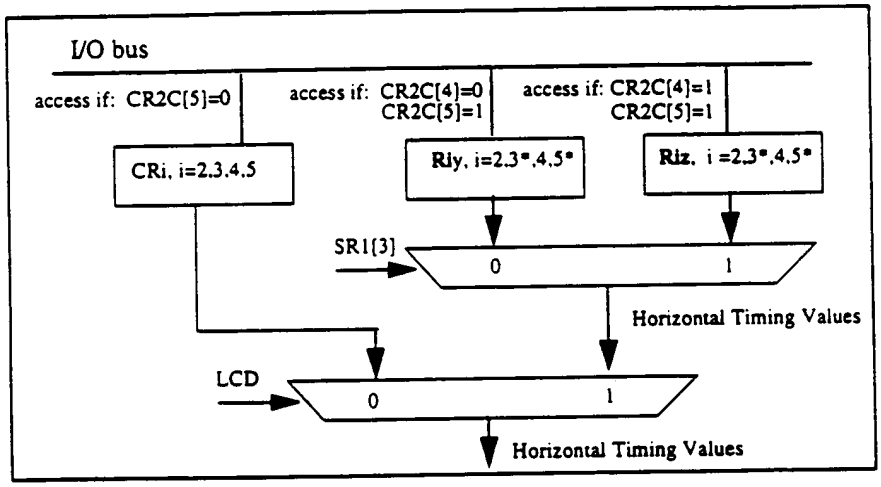
Bit	Definition
[3:2]	Most Significant Bits for RDx. Write protected by CR2D[7].
[1:0]	Most Significant Bits for RCx. Write protected by CR2D[7].

Bit	Definition
[7:6]	Shade Mapping 00 -> 18bit output of LUT upped to 24bit or direct/true color used for dithering and shading 01 -> green output of the combined 8bit data channel (LUT or True color) goes to dither and shader 10 -> Direct display of Attribute Palette address, bypassing dither ,going through shader. To be selected in text modes as well as one and two bit per pixel packed modes . Works with CR20[0] for text. 11 -> Pixel Address (6bit output of Attribute controller) bypasses dither to go to shader.
[5]	Reverse Video for Text Modes
[4]	Reverse Video for Graphics Modes
[3:2]	**Reserved**
[1]	**Text Contrast Enhancement. With R8X[4] defines the same matrix as in 62XX.**
[0]	**Enable Dithering (0=disable)**

CR2C - Flat Panel Interface Register (was CR1C in T1)

CL 158163

Bit	Definition
[7:6]	LCD Flat Panel Class Select 00 -> STN Mono Panel 01 -> grey scal plasma or EL 10 -> STN color panels 11 -> TFT color panels
[5] new	**Access Hoizontal Timing Shadow Registers Ry and Rz** **0= no access to horizontal shadow registers** **1= access both standard VGA horizontal timing and the horizontal shadow registers** **At any time, the shadow registers control the CRTC. In standard VGA on a CRT, this bit is 1 and what is written in VGA registers is also written in shadow register, so it looks as if standard VGA registers control the CRTC but they do not.**
[4] new	**In T1 this register enabled extra LLCLK for Epson panels — this feature is no longer needed in Nordic, so the bit changed function:** **SElect which set of horizontal timing shadow registers is accessed by CPU: y (normal) or z (for dot-clock divided by 2).** **0 -> Rly , i=0,2,3,4,5** **1 -> Rlz**



[3]	**Protect CRTC Registers for LCD**
[2]	**MCLK Suspend Mode Power Down**
[1]	**Invert LLCLK Control**
[0]	**Invert LFS Control**

3.5 CR2E - High-Resolution Panel Control Register

Bit	Definition
[7:6]	Actual Display Size 00 = VGA modes 01 = 800x600 actual display 10,11 = reserved for 1024x768 and 1280x1024 The value programmed in this registers affects the expansion mechanism on an 800x600 panel. If an 800x600 panel is selected at R9X[3:2] (=01) and CR2E[7:6]=01 then the expansion is disabled in graphics modes even if CR2E[3,1] expansion bits are on. With this mechanism the BIOS does not need to save the status of CR2E[3,1] every time it sets mode 800x600 so that it could restore when going back to 640x480 modes.
[5]	**Enable Horizontal Centering on Panels**: For 800 x 600 and 1024 x 768 panels
[4]	**Enable 10-dot true fonts.** Has effect only in text. Default = '0'; disabled
[3]	**Enable Horizontal Graphics Expansion** – that replicates each fourth pixel. Active only if the controller is in graphics mode. This expansion is used to expand 640 to 800 in 800 x 600 and 1024 x 768 panels. Default = '0'; disabled
[2]	**Enable Horizontal Expansion** – of an 8-wide true font to 10 dots instead of the normal VGA expansion which is to 9 dots. Has effect only in text mode. Default = '0'; disabled
[1]	**Enable Vertical Graphics Expansion**: For 800 x 600 panels: doubling of every odd scan-line in graphics in 350 and 400 line modes – replicate every forth line in 480 line modes. Default = '0';disabled When this bit = '1', and the controller is in graphics mode, the 800 x 600 expansion is enabled, and, depending on CR12 contents (with appropriate expansion bits in CR07), either odd line replication is enabled, or one line out of four replication is enabled. The comparizon with CR12 should be for smaller or equal!! This kind of expansion is used in 800 x 600 and 1024 x 768 panels when running VGA programs, and its purpose is to fill the screen as much as possible.
[0]	**Enable 800x600 panel text expansion:** Odd scan-line doubling (for 9 x 14 or 8 x 16 font) or every scan-line tripling (for 8x8 font). Default = '0'; disabled When this bit = '1', and the controller is in text mode, the odd scan-line replication is enabled. This kind of expansion is used in 800 x 600 and 1024 x 768 panels when running VGA programs and its purpose is to fill the screen as much as possible.

CR2F - Microsoft Windows Chip ID

Bit	Definition
[7:0]	Read only register. It reads back a code to remain the same for Nordic through its entire life. Any application like MS Windows or OS/2 should ID Nordic by reading this register. For Nordic the read-back code is "CDH".

4.0 TV-OUT Registers

4.1 CR30 - TV Out Control Register

Bit	Definition
[7:4]	Reserved
[3]	Configure Nordic and Enable the TV-OUT mode for Analogl Encoders This bit comes out on TV-ON pin If this bit is 0, NTSC/PAL pins and CSYNC pin are forced L
[2]	NTSC/PAL pin value if CR30[3] is 1 If CR30[3]=0, the value of this bit does not affect the NTSC/PAL pin.
[1:0]	Skew Control for CSYNC generation 00 = no skew 01 = skew by two dot-clocks on horiz sync start and one dotclock on half line for interlaced 10 = skew by four dot-clocks on horiz sync start and two dotclocks on half line for interlaced 11 = skew by six dot-clocks on horiz sync start and three dotclocks on half line for interlaced

5.0 Registers for Motion Video Architecture

5.1 CR34 - MVW XS Register

Bit	Definition
[7:0]	**MVW Horizontal Start Coordinate XS** (in surrounding pel depth memory cycles) The horizontal position is programmed with 8 pixel resolution (0,8,16,... pixels starting from the left side of the screen) (up to 1K pels in increments of 8 pels). To get an early warning, we will require **XS** to be programmed 8 pixels less than the actual position: 0 = zero, 1 = 16 pels, 2 = 24 pels, etc.

5.2 CR35 - MVW Horizontal Width XW Register

Bit	Definition
[7:0]	MVW Horizontal Width XW (MVW pel depth memory cycles) (up to 1K pels in increments of 8 pels). To get an early warning, we will require XW to be programmed 8 pixels less than the actual width: 0 = zero, 1 = 16 pels, 2 = 24 pels, etc. width.

5.3 CR36 - Vertical MVW High Position Register

Bit	Definition
[7]	Reserved
[6]	Cinepak type YUV to RGB conversion. If this bit = 0, YUV to RGB conversion is done according to the standard algorithm If this bit = 1, the YUV to RGB conversion is done based on Cinepak algoritm.
[5]	Excess 128 for YUV to RGB conversion. U and V are integer values expressed as two-th complement or excess 128. If this bit = 0, the YUV to RGB converter assumes that U and V are expressed in 2-th complement format (as in Philips SAA715B and SAA9051 TV Decoders). If this bit = 1, the YUV to RGB converter assumes that U and V are expressed in excess 128 format.
[4]	**MVW Memory Address Offset** (WMAdOf MSB)
[3:2]	**Vertical MVW End MSBs** (see CR37)
[1:0]	**Vertical MVW Start MSBs** (see CR38)

5.4 CR37 - Vertical MVW Start Register

Bit	Definition
[7:0]	**Vertical MVW Start YS**: (in true scan-lines not affected by scan-line doubling or panel vertical expansion) 10 bits in CR36[1:0] (msbs) and CR37[7:0] (lsbs).

5.5 CR38 - Vertical MVW End YE Register

Bit	Definition
[7:0]	**Vertical MVW End YE:** (all bits are programmed, in true scan lines) 10 bits in CR36[3:2] (msb-s) and CR38[7:0] (lsb-s).

5.6 CR39 - Surrounding Address Offset Register

Bit	Definition
[7:0]	**Surrounding Address Offset:** SAdOf (a number to be added every line to the surrounding CRT Address Counter value to allow it to jump over the MVW without counting through it. This allows calculating the surounding restart address.) This number depends on the surrounding mode resolution. Assuming a maximum line of 1024 pels, in increments of 4 pels per address (8-bits/pel), 256 addresses is enough for eight bits

5.7 CR3A - MVW Memory Address Start Register

Bit	Definition
[6:0]	**MVW Memory Address Start:** WMAdS in increments of 16KB = 4KW (a phisical address 00000:3FFFF for 1MB or 00000:7FFFF for 2MB Video Memory).

5.8 CR3B - MVW Memory Address Offset Register

Bit	Definition
[7:0]	**MVW Memory Address Offset** WMAdOf (A number to be added to the current MVW Start Address to get the next MVW start Address). Having this s/w model allows panning through a large image for the MVW. The actual image stored in memory may be as large as 2K pixels at 16 bits per pixel (two per word) -> 10bits. 10bits -> in CR36[5:4] (msb) and CR3B[7:0] (lsb).

5.9 CR3C - MVW Pixel Format Register

Bit	Definition
[7]	**MVW horizontal zoom** (doubling)
[6]	**MVW vertical zoom** (doubling)
[5]	**Enable Live Video in Full Screen**
[4]	**Enable Motion Video Window**
[3:0]	Encode format for the first Motion Video Window 0h = 0000 = 8 bit RGB 3:3:2 going through the palette 1h = 0001 = 16 bit RGB Sierra (5:5:5) 2h = 0010 = 16 bit RGB XGA (5:6:5) 3h = 0011 = 4:2:2 YUV Y0UY1V 4h = 0100 = 4:1:1 YUV linear Y0Y1Y2Y3UV 5h = 0101 = 4:1:1 YUV array Y0Y1Y2Y3UV but Y2Y3 are in next scan line 6h = 0110 = Sashapak 6 bits for U/L 7h = 0111 = Sashapak 8 bits for U/L 8h:Fh = 0111:1111 = reserved for future formats

5.10 CR3D - Motion Video Window Horizontal Size Register

Bit	Definition
[7]	**MVA Data Bus Signature Generation Selection bit.** **0 = selects VGA Data Path for signatire generation** **1 = selects MVA Data Path for signature generation**
[6:0]	Motion Video Wondow width in 8 pixel units This register is used to specify the horizontal width of the MVW in 8 dot-clock units. The MVW has to be a multiple of 8 pixels. The value programmed in this register is used to terminate the MVW on each scan line.

6.0 Registers for Panel Horizontal Timing Control

This set of four registers are used to generate horizontal panel timing with 640x480 or 800x600 panels and to center horizontally a 640dots or 720dots picture on an 800x600 panel.

6.1 CR40 - No Center Panel HDE Start Register

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. This register is used to program Panel Line Clock Start and Panel Display Enable Start with both 640x400 and 800x600 panels any time no horizontal centering is needed. Used automaticall y by h/w if CR41 and CR42 are not used.

6.2 CR41 - Panel HDE Start Register to Center 720 dots

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 720 dot mode (text or graphics - RIX mode only) is centered on an 800x600 panel. If horizontal expansion is on, CR40 is used. Used automatically by h/w if : 800x600 panel & No 800x600 graphics mode & 8 dot character clock & no horizontal expansion

6.3 CR42 - Panel HDE Start Register to Center 640 dots

Bit	Definition
[7:0]	Panel Horizontal Display Enable Start relative to previous HDE start, in 4 dot-clkock units. The dot-clock used is never divided by two. The value in this register will be automatically used by Nordic to control Panal Line Clock and Panel Horizontal Display Enable Start anytime a 640 dot mode (text or graphics) is centered on an 800x600 panel. If horizontal expansion is on, CR40 is used. Used automatically by h/w if : 800x600 panel & No 800x600 graphics mode & (9 dot character clock + horizontal display enable >= 50H) & no expansion no horizontal expansion

6.4 CR43 - Panel HDE Dot-Clock Skew Control Register

By programming this skew, it is possible to compensate internal delays on Panel HDE for diferent types of panels. If all delays are matched the skew fields should be zero to align with character clock.

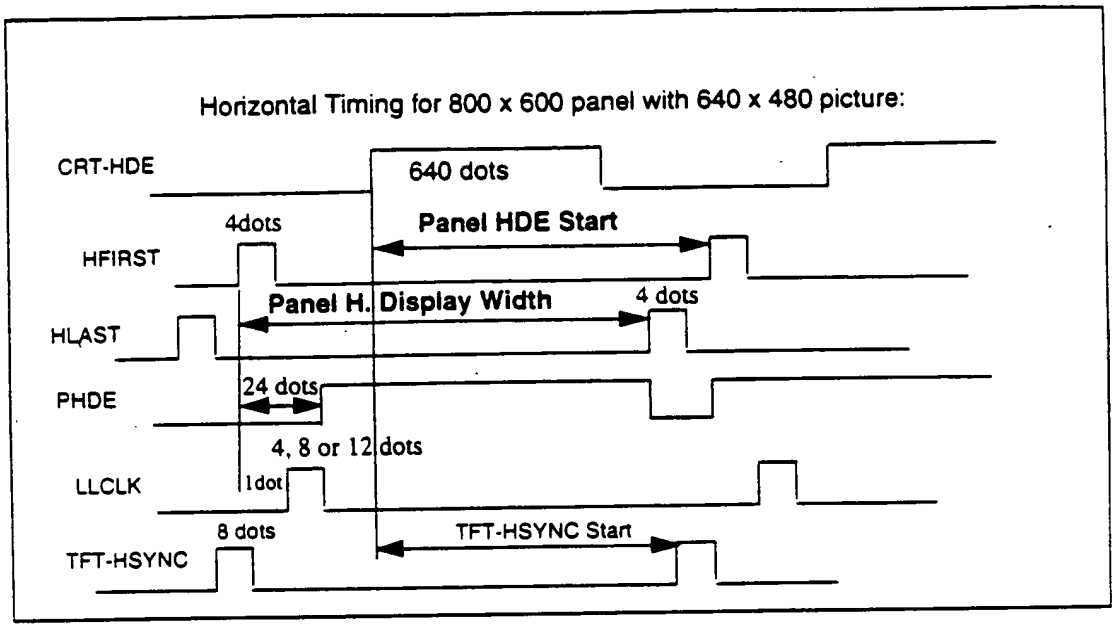
Automatic switching between these three registers will be done based on CRTC and Sequencer programming and the type of panel used
(640 x 480 or 800 x 600).

Bit	Definition
[7:6]	**Panel Line Clock Width:** '00' = 4 dot-clocks '01' = 8 dot-clocks '10' = reserved '11' = reserved
[5:4]	**CR42 value fine (dot-clock) skew:** '00' = no skew '01' = delay Panel HDE start by one dot-clock '10' = delay Panel HDE start by two dot-clocks '11' = delay Panel HDE start by three dot-clocks
[3:2]	**CR41 value fine (dot-clock) skew:** '00' = no skew '01' = delay Panel HDE start by one dot-clock '10' = delay Panel HDE start by two dot-clocks '11' = delay Panel HDE start by three dot-clocks
[1:0]	**CR40 value fine (dot-clock) skew:** '00' = no skew '01' = delay Panel HDE start by one dot-clock '10' = delay Panel HDE start by two dot-clocks '11' = delay Panel HDE start by three dot-clocks

6.5 CR44 Horizontal Panel Display Width Register

The value in this register is expressed in 4 dot-clocks (never divided by two).

Bit	Definition
[7:0]	Panel Display Width in hex expressed in four dot-clock chunks. As it is used to compensate or internal delays, this value is close but not exactly 640/4 or 800/4.



6.6 CR45 and CR46 are reserved registers. They are in the data base and can be used for future needs as control registers. They were put here in case we need one more set of horizontal registers for automatic switching between diferent modes.

CR47 - TFT HSYNC Horizontal Position Register

TFT HSYNC is about 144 dot-clocks ahead of Panel Display Enable Start. This register allows to program the exact position in dot-clock/4 from CRT-HDE start to TFT HSYNC Start. This set-up is independent of character clock width and dot-clock divide by two control. TFT HSYNC pulse width is 8 dot-clkocks.

Bit	Definition
[7:0]	TFT HSYNC start position in doc-clock/4, relative to actual panel horizontal display enable start.

6.7 CR48 - TFT HSYNC and Panel Height Overflow Register

Bit	Definition
[7]	Reserved
[6]	Reserved for 1024 panels
[5:4]	Bits 9 and 10 of CR4A (Single Scan Panel Size and Dual Scan Lower Panel Size)
[3]	Reserved for 1024 panels
[2]	Bit 9 of CR49 - mid dual scan panel size (upper half size in scan-lines)
[1:0]	TFT HSYNC dot-clock skew 0:3 This register allows to position TFT HSYNC with dot-clock resolution.

6.8 CR49 - Dual STN Panels Upper Half Vertical Size Register

Bit	Definition
[7:0]	Least Significant 8 bits of the Upper Half Vertical Size (in scan lines). This is relative to the start of the Vertical First pulse - the start of the panel vertical display, which in centering is ahead of the actual vertical display. Bit 9 is CR48[2]. This allows up to 511 lines to be displayed in the upper half. Please note that this are actual displayed lines (unlike the extra lines programmed in CR4B. Program mid -1 in this register (239lines programmed for 240 lines displayed).

6.9 CR4A - Dual STN Panels Lower Half Vertical Size Register

Bit	Definition
[7:0]	Least Significant 8 bits of the Lower Half Vertical Size as well as of the Single Scan Panel Vertical Size (in scan lines). This is relative to the start of the Vertical Mid (dual-scan) or First (single scan) pulse. Bits 10 and 9 are in CR48[5:4]. This allows up to 1024 lines to be displayed in the upper half. Please note that this are actual displayed lines (unlike the extra lines programmed in CR4B. Normally the two panel halfs have the same number of scan-lines. Program last -2 in this register (478 programmed for 480 lines panel).

6.10 CR4B - Extra Line Clocks Register

Bit	Definition
[7:4]	Extra Line Clocks added in the Upper Half 0:15 By adding extra line clocks, panel generated MOD will be affected. This register should be 0 in simulscan. The line clocks added are off by one actual scan-line.
[3:0]	Extra Line Clocks added in the Lower Half 0:15 By adding extra line clocks, panel generated MOD will be affected. The line clocks added are off by one actual scan-line.

CR4C - Input Resolution Override Register for Dithering

Bit	Definition
[7]	Enable Input Resolution Override (default disable) Normally the graphics mode resolution is decoded and fed to the dither block. For all graphics modes that go through the RAMDAC RAM - 6bits/gun is automatically the input resolution. For 5:5:5 RGB or 5:6:5 RGB or 8:8:8 RGB we use a diferent input resolution: 5 for 5:5:5 and 5:6:5 and 8 for 8:8:8 RGB. In all cases the proper input resolution is automatically selected. If there is a need to overide this value, than we wiill use this bit to enable the override and write the new value in bits 3:0. For 8 bit per gun we write 8 (1000), for 6 bits per gun -> 6 (0110) and for 5 bits per gun -> 5 (0101).
[6:4]	Reserved
[3:0]	The binary value of the override input resolution. 1000 -> 8bit/gun 0110 -> 6bit/gun 0101 -> 5bit/gun

CR4D - Output Resolution Register for Dithering

Bit	Definition
[7:4]	Reserved
[3:0]	The binary value of the output resolution for dithering 1000 -> 8bit/gun (TFT) 0110 -> 6bit/gun (TFT) 0100 -> 4bit/gun (TFT or 16 shades STN) 0011 -> 3bit/gun (TFT or 8 shades STN) 0010 -> 2bit/gun (4 shades STN) 0001 -> 1bit/gun (2 shades STN)

7.0 Registers for the AUDIO of NORDIC-1M.

7.1 GR60 Wave Port Control 1

Bit	Definition
[7]	Reserved
[6]	Reserved
[5]	Enable audio for host accesses.
[4]	Select 4215
[3]	Stereo for reciever (i:e STEREO CODEC)
[2]	Stereo for transmitter (i:e STEREO NORDIC)
[1:0]	Data Format select '00' 16 bit '01' 8 bit '10' 4 bit '11' reserved.

7.2 GR61 Waveport control 2

Bit	Definition
[7]	Reserved
[6]	**Power-down Conttrol:** '0' will force 'low' on PDN.
[5]	**Enable command mode.** The 4215 Audio Controller must have been placed in COMMAND mode by forcing 'low' on D/C* pin.
[4]	**Input level in SDI:** in command mode.
[3]	**Output level on SDO:** in command mode.
[2]	**Output level on SCLK:** in command mode.
[1]	**Output level on FSYNC:** in command mode.
[0]	**Output state of D/C* pin.**

7.3 GR62 - Input Audio Threshold setting.

Bit	Definition
[7:0]	Available only for 16-bit mode. Only +VE data is compared; i.e. if msb of left data is '1', no compare is performed.

7.4 GR65

Bit	Definition
[7]	Enable Threshold detect mode.
[6:0]	Reserved

7.5 GR66 - Audio Input Codec Write Pointer - high byte

Bit	Definition
[7:0]	Audio Input Codec write pointer - high byte

7.6 GR67 - Audio Input Enable and Codec Write Pointer - low byte

Bit	Definition
[7]	Enable input from codec to audio buffer.
[6:0]	Audio Input Codec Write Pointer (low 7 bits of 15 bit pointer)

7.7 GR6A - Audio Output Codec Read pointer - high byte

Bit	Definition
[7:0]	Audio Output Codec Read pointer high byte

7.8 GR6B - Audio Output Codec Read pointer low byte

Bit	Definition
[7]	Enable output to codec from audio buffer.
[6:0]	Audio Output Codec read pointer (low 7 bits of 15 bit pointer).

7.9 GR6C - Interrupt Control.

Bit	Definition
[7:6]	Reserved.
[5]	Standard VGA Interrupt disable. '0' = Allow VGA interrupt '1' = Disable VGA interrupt.
[4:2]	Reserved.
[1]	Audio Input interrupt control ----> DURING RECORD SESSION. '0' = Disable this interrupt source. '1' = Enable input buffer full OR programmed full interrupts.
[0]	Audio Output interrupt control ----> DURING PLAY SESSION. '0' = Disable this interrupt source. '1' = Enable Output buffer empty OR programmed empty interrupts.

7.10 GR6D - Interrupt Status.

Indicates any active enabled interrupt. Reading this register will clear the interrupt state and reset the status. No effect on the standard VGA interrupt status or interrupt. For all of the following bit positions, a '1' in the bit means PENDING INTERRUPT.

Bit	Definition
[7:6]	Reserved.
[5]	Standard VGA Vsync interrupt (state of 3C2(7)).
[4]	Reserved.
[3]	Record Buffer FULL (OVERRUN).
[2]	Record Buffer PROGRAMMED FULL.
[1]	Play Buffer EMPTY. (UNDERRUN)
[0]	Play Buffer PROGRAMMED EMPTY.

7.11 GR6E - AUX1 and AUX2 control

Bit	Definition
[7]	Enable Aux Sel 1 low-true output on adress match 530-53Fh.
[6]	Enable Aux Sel 2 low-true output on adress match 388-397h.
[5:0]	Reserved.

7.12 GR6F - Codec status.

Bit	Definition
[7:4]	Reserved
[3]	Timer status (ADI) time slot 6 bit 7
[2]	Overrange (OVR) time slot 7 bit5
[1]	PIO1 input status. time slot 7 bit 7
[0]	PIO0 input status. time slot 7 bit 6

7.13 GR70 - Codec control DWORD from Nordic to codec. byte D7:0

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D7:0

7.14 GR71 - Codec control DWORD from Nordic to codec. byte D15:8

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D15:8

7.15 GR72 - Codec control DWORD from Nordic to codec. byte D23:16

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D23:16

7.16 GR73 - Codec control DWORD from Nordic to codec. byte D31:24

Bit	Definition
[7:0]	Codec control DWORD from Nordic to codec. byte D31:24

7.17 GR74:75 - Interrupt value for audio IN buffer.

Bit	Definition
[7:0]	Interrupt value for audio IN buffer. When the CODEC reaches the programmed adress -1, an interrupt is generated during the record session.

7.18 GR76:77 Interrupt value for audio OUT buffer.

Bit	Definition
[7:0]	Interrupt value for audio OUT buffer. When CODEC read pointer reaches the programmed adress -1, an interrupt is generated during the play session.

8.0 Registers that Overlap in T1 and AVGA3, now moved to other locations.

8.1 CR1B[7,4:2] - Bits are Reserved in Nordic

Bit	Definition
[7,4:2]	R1B in schematics All these bits do not seem to be actually used. I do not think that they are needed in Nordic.

8.2 CR1C(T1) - Moves to CR2C

8.3 CR1D(T1) - Moves to CR2D

8.4 SR7(T1) [6:4] Not used, keep the function of AVGA3.

8.5 SR8(T1) - Moves bits as follows:

Bit	Definition
[7]	moved to SR23[7] but with reversed polarity (assymtric DRAM)
[6]	remains in SR8[6] (disable MCS16* for Video Memory)
[3]	Reserved in Nordic - Suspend inpout is active 'high' (no selectable active polarity like in T1)
[2:0]	moved to SR24[2:0] (SW2:0 read-back)

8.6 SRF[7](T1) - Not used, becomes a constant '0'.

8.7 SR16(T1) - Moves to SR20; Pads Threshold and Power Control

8.8 SR1A(T1) - Moves to SR21 Test Register, in case it is needed.

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9.0 Register Bits of AVGA3 which are not used in Nordic

The following register bits are not used in Nordic, though they are in AVGA3 data base. In most cases (if not specified otherwise) they can be taken out together with the logic related to them. When specified, they will be preserved in the data base together with the related logic.

9.1 SR8[7,5:0] - Used for EEPROM programming - not a Nordic feature

9.2 GRE[0] - DCLK/2 to Feature Connector

10.0 Register Bits in T1 not used in Nordic

10.1 SR7[6:4]

Switch read back from MD pull-ups in 486 bus, is not used in Nordic. SR7 will have the same function as in AVGA3.

10.2 SR8[3]

Supend Input active polarity in T1. This is not used in Nordic, since in Nordic SUSPI is always active 'high' polarity.

10.3 SRF[1:0]

MCLK frequency select in T1 are not used in Nordic: only SR1F is used. See new definition of SRF.

10.4 CR1C[2:0]

"MCLK Suspend mode power down", "Invert LLCLK", "Invert LFS" are not used in Nordic. Instead, Nordic will always stop MCLK and VCLK in Suspend, and will have a positive polarity on LLCLK and LFS.

11.0 Register Bits with Similar, but Different, Functionality in Nordic vs. T1

11.1 CR20[2:1] - Refresh Select

Refresh Select is almost the same in Nordic as in T1, but, when '11', not only RAS and CAS are set to high-impedance, but all Nordic outputs going to the Memory (MA, MD, WE, OE, CAS, RAS) are set to high-impedance. To be used with NEC's GDC option.

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